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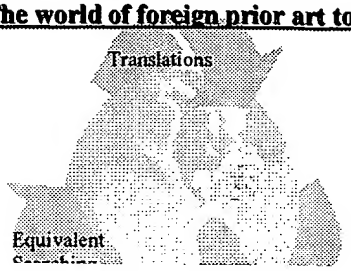

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HIGH BREAKDOWN STRENGTH SEMICONDUCTOR DEVICE

(Ko Taiatsu Handotai Sochi)

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UNITED STATES PATENT AND TRADEMARK OFFICE

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/1[1]

(54) [Title of the Invention]

High Breakdown Strength Semiconductor Device

(57) [Abstract]

[Purpose] To prevent a decline in breakdown strength caused by the stretch bending of a depletion layer due to a charge induced on a field plate in a high breakdown strength semiconductor device provided with guard rings and the field plate.

[Constitution] A charge induced by a field plate is relieved to a main electrode via a low-resistance film of sheet resistance 10^8 - 10^{11} by covering the field plate with the low-resistance film. The occurrence of cracking on the low-resistance film due to a downward stress is prevented by laminating a stress absorbable insulating film on the low-resistance film. A silicon nitride film which can be formed by adjusting the specific resistance according to a plasma CVD process can be effectively used for the low-resistance film.

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[1]Numbers in the margin indicate pagination in the foreign text.

[Claims]

[Claim 1] A high breakdown strength semiconductor device wherein main electrodes are provided on two principal faces of a semiconductor substrate, guard ring regions of same conduction type as a region contacting with the main electrode of one face are selectively formed on the surface of said substrate from said region to the edge side made to same potential as the main electrode of the other face and contacted with the surface of said region contacting with said main electrode and the guard ring regions, and a field plate made of an oxide film extending to said edge side is arranged on the substrate surface, characterized by covering the field plate with a low-resistance film of sheet resistance 10^8 - 10^{11} Ω/□.

[Claim 2] A high breakdown strength semiconductor device, wherein a stress absorbable insulating film is laminated on the low-resistance film in the device described in Claim 1.

[Claim 3] A high breakdown strength semiconductor device, wherein the low-resistance film is a silicon nitride film formed by a plasma CVD process in the device described in Claim 1 or 2.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application] The present invention relates to a high breakdown strength semiconductor device having a

guard ring structure for making a high breakdown strength.

[0002]

[Prior Art] In order to make a semiconductor device to have a high breakdown strength, a depletion layer of substrate surface must easily extend to the transverse direction and the electric field strength must be reduced by designing a pattern of chip surface of said semiconductor device or a diffusing layer, etc. as well as the specific resistance of said substrate is increased and the depletion layer easily extends to the inside of substrate. Particularly, the higher the breakdown strength, the more important the guard ring structure at the periphery of a chip will be, thus it is so designed that the depletion layer is easily extended by increasing P diffusion rings and lengthening the field plate. Fig. 2 shows a part of a vertical MOSFET in one example of such a high breakdown semiconductor device,a P-type diffusion layer **2** is formed on a N-type silicon substrate **1**, a drain electrode **3** contacts with the substrate **1** and a source electrode **4** contacts with the P layer **2**. the P layer **2** is enclosed and P-type guard ring regions **5** are formed by diffusion simultaneous with the P layer are arranged in two stage, and an N channel stopper region **6** is formed at the edge of said substrate **1**. Al wires contact with the guard ring regions **5** and the channel stopper region **6**. A field plate layer **8** made of SiO_2 covers the substrate **1** between the source electrode **4** and the Al wires **7**, between the Al wires **7** and from the Al wires **7** to the channel stopper region **6**. Then, a passivation film **9** for stabiliza-

tion covers on the Al wires **7** and the field plate layer **8**, and a surface protective material **10** further covers thereon, including the side of substrate **1**, to prevent the invasion of moisture from the external.

[0003]

[Subject to Be Solved by the Invention] However, if semiconductor chips thus designed for making a high break-down strength are used to assemble a semiconductor device and then measure the breakdown strength, the value becomes lower than the state of chips. Particularly, the higher the breakdown strength, the greater this difference. This is because the charge of a gel or a surface protective material called JCR which is coated on the chip surface during the assembly to protect the surface from the moisture, etc. induces a charge on the chip surface. Particularly,a charge induced on a field plate of guard ring part affects as far as the chip surface and stops the extension of a depletion layer, consequently the breakdown strength is lowered.

[0004] If this is illustrated in Fig. 2 and if an inverse voltage is applied to a joint between a P layer **2** and an N-type substrate **1** with a drain electrode **3** as positive and a source electrode **4** as negative, depletion layers **11** occur. The extension of said depletion layers **11** into the N-type substrate is shown by dotted lines in the figure. The depletion layers **11** are easy to extend in the transverse direction due to an effect of guard rings **5** and the breakdown strength also smoothly rises with increasing a

voltage between the drain electrode **3** and the source electrode **4**. However, the charge in the surface protective material **10** exerts an influence on the surface of said substrate **1** under a passivation film **9** and a field plate layer **8**, the stretch of said depletion layers **11** is bent as shown by a dashed line **12**. This bending is strengthened with raising the voltage, and the depletion layers **11** break down here in the end. Therefore, a problem of breakdown strength decline arises.

[0005] The breakdown strength must be raised only by the decline part in the chip step to compensate the decline. As formerly described, the width of guard rings must be expanded and the specific resistance of said substrate must be increased for raising the breakdown strength, but the chip dimensions increase and the cost rises if the width of guard rings is expanded. Moreover, if the specific resistance of said substrate is increased, a problem of increasing the resistance of said device was present. Furthermore, if the specific resistance of said substrate is increased, such an adverse effect that the substrate is also easily affected by the charge of said surface protective material.

[0006] Still more, the deterioration of reliability caused by the occurrence of cracking on a semiconductor chip itself or a passivation film on its surface due to a stress from a container for receiving the chip or the surface protective material is given as another problem. Therefore, it was necessary to use an insulating layer such as SiO_2 or PSG (polysilicon gate) formed at especially

low temperatures for the relaxation of said stress.

[0007] The purpose of present invention consists in solving the above problem and providing a high breakdown strength semiconductor device which prevents a breakdown strength decline caused by the stretch bending of a depletion layer, needs not to increase the specific resistance of substrate or expands the width of guard rings or further solves the problem of cracking occurrence.

[0008]

[Means for Solving the Subject] To achieve the above-mentioned purpose, the present invention is made by covering a field plate with a low-resistance film of sheet resistance 10^8 - 10^{11} Ω/□ in a high breakdown strength semiconductor device wherein main electrodes are provided on two principal faces of a semiconductor substrate, guard ring regions of same conduction type as a region contacting with the main electrode of one face are selectively formed on the surface of said substrate from said region to the edge side which is made to same potential as the main electrode of the other face and contacted with the surface of said region contacting with the main electrode and the guard ring regions, and a field plate made of an oxide film extending to said edge side is arranged on the substrate surface. Moreover, it is effective that

/3

a stress absorbable insulating film is laminated on that low-resistance film. Then, it is effective that the low-resistance film is a silicon nitride film formed by a plasma CVD process.

[0009]

[Functions] Since the charges of said surface protective material, etc. can be relieved to the main electrode via the low-resistance film, the depletion layer can smoothly stretch under the field plate to improve the breakdown strength. When the resistance of said low-resistance film is too low, however, it is feared that a leakage current flowing from the edge of substrate, which is made to same potential as the main electrode of the other face, to the main electrode of one face via the low-resistance film increases, the loss increases and a heat generation taking the low-resistance film as a resistor occurs, thus the semiconductor substrate breaks down. The sheet resistance 10^8 - 10^{11} Ω/□ is an appropriate range decided from these conditions. However, many materials of said low-resistance film are hard materials unfit to the stress relaxation, in addition, if a stress absorbable insulating film is laminated, cracks coming into the low-resistance film can be prevented by a stress applied from the upper members such as the surface protective material or container, etc. Even if the cracks come into the conductive layer, contaminants from the external can be prevented by the insulating film. Moreover, even if defects such as pinholes, etc. occur on the low-resistance film and the insulating film, it is effective on the invasion of moisture, etc. from the external because the defects of said low-resistance film and said insulating film do not superimposed in same positions.

[0010]

[Actual Examples] Fig.1 shows a vertical type MOSFET of one actual example of the present invention. Same symbols are attached to parts common to Fig. 2. A semiconductor substrate is same as Fig. 2, but a 1,000 Å-thick low-resistance film **21** consisting of P-SiN is covered on Al wires **7** and a field plate layer **8** by a plasma CVD process. Moreover, an insulating film **22** consisting of SiO_2 or PSG formed at low temperatures is covered on the low-resistance film **21**. The semiconductor substrate having such a surface structure is received in a resin container **23**, and a surface protective material **10** such as a joint covering resin (JCR) is filled in the space. The specific resistance of material P-SiN of said low-resistance film **21** can be adjusted by changing the mixing ratio of reaction gases SiH_4 to NH_3. If the ratio of SiH_4 is increased, the x of composition Si N increases to reduce the resistance; if the ratio of NH_3 is increased, the y of composition Si N increases to increase the resistance or become insulative. Fig. 3 shows an invert breakdown strength of a MOSFET fitted with a low-resistance film **21** of various sheet resistances and aimed at a breakdown strength of about 1,300 V and a leakage current between drain/source electrodes **3**, **4**. If the sheet resistance is made to 10^{10} Ω/□ or above, the breakdown strength reduces from the objective 1,300 V by subjecting to an effect of charge of said surface protective material **10** and the leakage current rises at a sheet resistance of below 10^9 Ω/□. Accordingly, it is desirable to control the film quality and the film thickness so as to come into this range, but

the film-forming is easy and practical characteristics are obtained if the sheet resistance is in a range of 10^8 - 10^{11} Ω/□. Then, the low-resistance film **21** works with the insulating film **22** as a passivation film.

[0011] Silicon is deposited as the low-resistance film **21** by vapor deposition process, sputter process or plasma CVD process, made to a polycrystalline or amorphous film, and a film with a specific resistance adjusted by the state of crystal or the quantity of added impurities. A film formed by coating a corresponding conductive resin by spin-on-glass (スピンオングラス) process, etc. may also be used. The depletion layer stretches as shown by a line **13** in Fig. 1 and a high breakdown strength semiconductor device having a breakdown strength as designed can be obtained by making the sheet resistance to 10^8 - 10^{11} Ω/□ although the low-resistance film is prepared by any processes.

[0012] As the insulating film **22**, a material which is softer than the low-resistance film **21**, useful for the stress relaxation from the surface protective material **10** or the container **23** as well as has a high moisture resistance effective to moisture invading from the external, e.g., SiO_2 or PSG formed at low temperatures, etc. may be used. However, the ratio of NH_3 in the formation of P-SiN by plasma CVD may be increased to make it high-resistance and thicken the film thickness of said low-resistance film **21** to, e.g., 8,000 Å so as to have said sheet resistance and fully absorb the stress without using the insulating film **22**. A low-resistance film

21 capable of covering parts with severe step, such as ethcing tapers of Al wires of substrate surface, may also be formed by fully thickening the film thickness.

[0013] When the insulating film **22** is formed, as illustrated, the low-resistance film **21** in a part A between a gate electrode **25** contacting with a gate **24** and the source electrode **4** can be removed by photoetching, and the gate electrode and source electrode can also be protected by allowing the insulating film **22** to lie between them. However, if the low-resistance film **21** remains in the part A, it can also be used as a protection circuit of a gate oxide film **26**. Namely, although a static electricity induced by human body, etc. flows into the gate electrode and damages the gate oxide film **26**, the static electricity coming into the gate **24** can also be relieved to the source electrode **4** by arranging the low-resistance film **21**.

[0014]

[Effects of the Invention] The present invention enables to prevent the effect of charges of the surface protective material, etc. on the low-resistance film, etc. on the stretch of said depletion layer in a direction parallel to the surface of semiconductor substrate by forming a low-resistance film of sheet resistance, e.g., with a resistance adjustable P-SiN film 10^8 - 10^{11} Ω/□ on the field plate layer made of silicon oxide and enables to make a high breaking strength of semiconductor device without especially increasing the specific resistance of substrate. Then, the present

invention enables to prevent the occurrence of cracking due to a stress applied from above members to the low-resistance film by laminating the stress absorbable insulating film on the low-resistance film.

[Brief Description of the Drawings]

[Fig. 1] Sectional view of principal parts of vertical type MOSFET in one actual example of present invention

[Fig. 2] Sectional view of principal parts of prior vertical type MOSFET

[Fig. 3] Diagram of relationships between sheet resistance of low-resistance film and characteristics of vertical MOSFET

[Description of the Symbols]

1 N-type silicon substrate

/4

2 P layer

3 drain electrode

4 source electrode

5 p guard ring region

7 wire

8 field plate layer

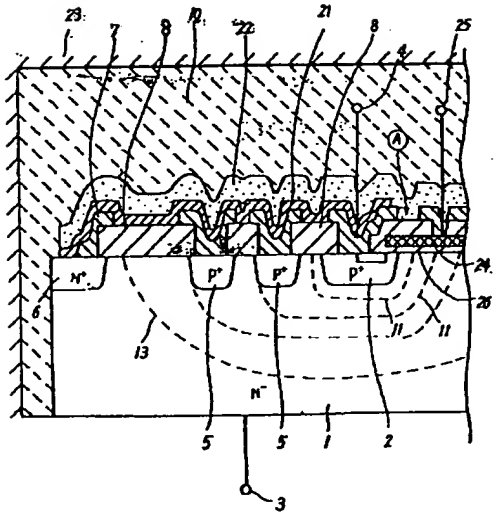
10 surface protective material

21 low-resistance film

22 insulating film

24 gate

[Fig. 1]



1 N-type silicon substrate

2 P layer

3 drain electrode

4 source electrode

5 guard ring region

7 wire

8 field plate layer

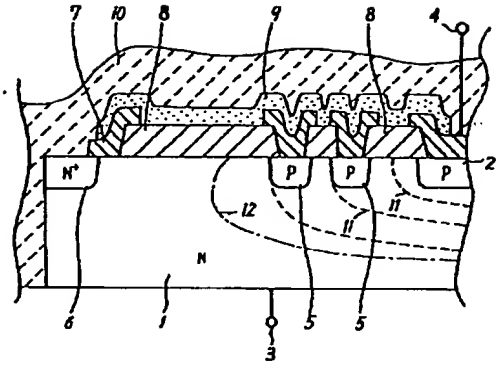
10 surface protective material

21 low-resistance film

22 insulating film

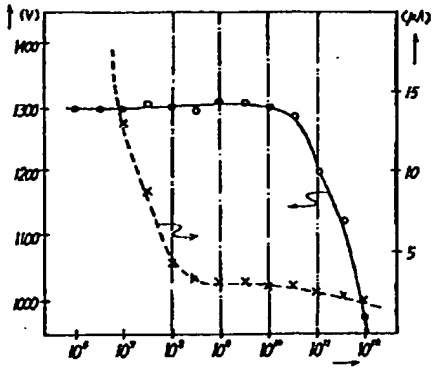
24 gate

[Fig. 2]



[Fig. 3]

Breakdown strength (V)



Leakage current (μA)

Sheet resistance of P-SiN film (Ω/□)